UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,410	09/16/2004	Ling-Wei Ke	MTKP0079USA	5409

27765 7590 05/05/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
COX, CASSANDRA F	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,410	KE, LING-WEI	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *32-42* is/are allowed.

6)☒ Claim(s) *1-9,13-14,17,19,22,26,29,43,48* is/are rejected.

7)☒ Claim(s) *10-12,15,16,18,20,21,23-25,27;28,30,31,44-47,49 and 50* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments with respect to claims 1-10 and 13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (U.S. Patent No. 6,760,397).

In reference to claim 1 Wu discloses in Figure 5 a method for changing a selectable divisor in a programmable frequency divider (500), the frequency divider comprising a plurality of cascaded cells (120, 130, 140), the method comprising: (a) providing a plurality of divisor signals (Pg<n>); (b) selectively switching each of the plurality of cells to a divide- by-two or a divide-by-three mode according to the plurality of divisor signals (see column 1, lines 25-38, where Wu discloses that the divider can be designed to divide by 2 or 3)); and (c) synchronously resetting at least a part of the plurality of cells (this is seen to be done by signal PgLoad).

In reference to claim 2 Wu discloses wherein in step (c) further comprise synchronously resetting all of the plurality of cells (this is seen to be done by the PgLoad signal; see Figure 5). The same applies to claims 3-4, 7, and 9 wherein this step also allows reloading of the plurality of divisor signals.

In reference to claim 5, Wu discloses in Figure 5 wherein the plurality of cells comprises at least one cell (130, 140) having a bypass mode (Zi), the method further comprising: determining whether to bypass at least a part of the at least one cell (301) having a bypass mode according to the plurality of divisor signals in order to inhibit bypassed cells from performing a frequency-dividing operation.

In reference to claim 6, Wu discloses in Figure 5 wherein step (c) further comprises synchronously resetting each bypassed cell (PgLoad). The same applies to claim 8 wherein this step also allows reloading of the divisor signals.

In reference to claim 13, Wu discloses in Figure 5 wherein step (c) further comprises bypassing a cell (301) having a bypass mode when divisor signal input to the cell and each of its subsequent cells having a bypass mode are a logic 0.

In reference to claim 14, Wu discloses in Figure 5 a programmable frequency divider (500) for dividing the frequency of a source signal (In) according to a selectable divisor which is obtained based on a plurality of divisor signals (Pg<n>) and outputting a result signal having a divided frequency, the programmable frequency divider comprising: at least one cell (120, 130, 140) of a first type being switchable between divide- by-two and divide-by-three modes having a first input node (C), a second input node (Min), a third input node (Pg), a fourth input node (Pc) , a first output node (Q) ,

and a second output node (Mo) , the third input node (Pg) being used for receiving a corresponding divisor signal, the fourth input node (Pc) being used for receiving a reset signal (PgLoad) to synchronously reset the cell of the first type; wherein if the programmable frequency divider comprising a plurality of cells of the first type, the cells of the first type being cascaded with each other , the first output node (Q) being coupled to a first input node (Q) of a subsequent cell of the first type, the second input node (Min) being coupled to a second output node (Mo) of the subsequent cell of the first type, a first input node (Q) of a first cell of the first type being coupled to the source signal (In), and a second input node (Min) of a last cell (J-last) of the first type being set to logic 1; the programmable frequency divider synchronously resets all of the cells of the first type according to the reset signal (PgLoad) in order to selectively switch each cell of the first type to perform a divide-by-two or divide-by-three operation according to the respective divisor signal (Pg<n>) after the cell is reset, and the second output node (Mo) or the first output node (Fo) of the last cell of the first type outputs the result signal having the divided frequency. The same applies to claim 22 wherein the fourth input node is used to receive a reload signal (PgLoad, which is seen to be equivalent to the reset signal). The same applies to claims 17 and 26 wherein the circuit further includes a cell of a second (or fifth) type (140) having a bypass mode and being cascaded to the last cell of the first type (120), the cell of the second type including all the inputs of the cell of the first type (120, as listed above) and a fifth input node (Zi), the fifth input node (Zi) being used to receive the last divisor signal (Pg<8>), wherein the cell of the second type (140) switches to the divide-by-two or the divide-by-three mode according to the

divisor signal (Pg<n>) received on the third input node (Pg) after being reset (by PgLoad), and if the last divisor signal (Pg<8>) received on the fifth input node (Zi) is at a bypass-mode active state, the cell of the second type switches to a bypass mode. The same also applies to claims 19 and 29, wherein the divider further comprises at least one cell of a third (or sixth) type (130) having the same inputs as the cell of the second type (140) as listed above and having a bypass mode and being cascaded between at least one cell of a first type (120) and the cell of the second type (140), wherein the cell of the third type functions (as claimed) similarly to the cell of the second type disclosed above).

In reference to claim 43, the claim is rejected for the same reasons as claims 14 and 17 above, wherein the cell of the tenth type is equivalent to the cell of the first type (120) and the cell of the eleventh type is equivalent to the cell of the second type (140).

Claim 48 is rejected for the same reasons as claims 19 and 29 above, wherein the cell of the twelfth type is equivalent to the cell of the third type (130).

Allowable Subject Matter

4. Claims 32-42 are allowed.

5. Claims 10-12, 15-16, 18, 20-21, 23-25, 27-28, 30-31, 44-47, and 49-50 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: Claims 10-12, and 21 would be allowable because the closest prior art of record

fails to disclose a method utilizing a control circuit coupled to each of the plurality of cells for providing a reset signal in combination with the rest of the limitations of the base claims and any intervening claims. Claims 25, 28, 31, 47, and 50 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 8 wherein the reload signal (RI) is provided by the second output node of the last cell of the fourth/tenth type (Fout) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 15-16, 18, 20, 23-24, 27, 30, 44-46, and 49 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 12 wherein the circuit operates as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims.

7. The following is an examiner's statement of reasons for allowance: Claims 32-42 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 12 wherein the divider has a reset node (Rs) and a reload node (RI) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

Cassandra Cox

April 30, 2006